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10/574,120	05/31/2007	Michel Bruel	5310-09500	7416
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MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL, P.C. P.O. BOX 398 AUSTIN, TX 78767-0398			EXAMINER KHARE, ATUL P	
			ART UNIT 1791	PAPER NUMBER
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/574,120	BRUEL, MICHEL	
	<b>Examiner</b>	<b>Art Unit</b>	
	ATUL KHARE	1791	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 24 November 2009.

2a) This action is **FINAL**.                    2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-20 and 29-33 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1-20 and 29-33 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All    b) Some \* c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date <u>07/06/2007</u> .	5) <input type="checkbox"/> Notice of Informal Patent Application
	6) <input type="checkbox"/> Other: _____ .

## DETAILED ACTION

### ***Election/Restrictions***

1. Applicant's election without traverse of Group I, claims 1-20 and 29-33 in the reply filed on 24 November 2009 is acknowledged.
2. Claims 21-28 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 24 November 2009.

### ***Specification***

3. The disclosure is objected to because of the following informalities: Borosilicate glass should be added to the specification at page 3 lines 20-23, page 5 lines 23-25, and page 8 line 30 to page 9 line 2.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
5. Claims 8-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. As to claim 8, the claim requires the addition of

boron **or** phosphorus. The claim does not cite the addition of boron **and** phosphorus.

The additive boron in a silica material creates borosilicate glass, and the additive phosphorus in a silica material creates phosphosilicate glass. For the purposes of further examination, the claim will be interpreted to require “phosphorus, boron, or combinations thereof” and “phosphosilicate glass, borophosphosilicate glass, or borosilicate glass”.

### ***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-4, 7, 8, 12, 14, 18, 20, 31, and 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Moriceau et al. (WO 99/35674). For the purposes of examination, (US 6,756,286) will be used as an English Language Equivalent.

8. As to claims 1-3, 31, and 33, Moriceau teaches in a method for transferring a thin film: forming a layer of inclusions in an initial substrate at a depth corresponding to the required thickness of the film (abstract). The inclusions are designed to form traps for gaseous compounds which are subsequently implanted to (irreversibly) form micro-cavities and form a fracture plane along which the thin film can be separated from the remainder of the substrate (abstract). In one example for obtaining an SOI structure, on

an initial substrate 31, a silicon film 32 (an intermediate layer), strongly doped with boron (extrinsic) atoms, is produced by epitaxy (column 12 lines 40-45, column 5 lines 10-12, figure 7). The substrate is then coated with an oxide film 34 (column 12 lines 45-50). The substrate is then submitted to gaseous compound implantation (column 12 lines 51-54). The surface 35 of the substrate is bonded by (molecular) wafer bonding to a silicon plate (a superstrate) (column 12 lines 55-57). Heat treatment is then performed to separate the structure 30 into two parts by means of a fracture at the inclusions zone in film 32 (column 12 lines 58-64). The presence of the (extrinsic) boron atoms implicitly causes the formation of micro-cavities (column 5 lines 20-21 and 30-33), and since the heat treatment induces fracture (weakening, rupture) of the substrate, it helps propagate (and further form) any cavities formed during the implantation step. Since micro-cavities are formed in film 32, and since film 32 is comprised of similar materials used by applicant as the intermediate layer, it is plastically deformable in the heat treatment range as required by the claims. The micro-cavities formed by this process implicitly constitute channels as required by the claims. The Moriceau process provides a structure that is suitable for the intended uses recited in claim 33.

9. As to claim 4, Moriceau teaches that subsequent to heat treatment, mechanical stresses can be used to cause separation of the substrate (column 4 lines 42-44).

10. As to claims 7, 8, 12, 14, 18, and 20, Moriceau teaches in a method for transferring a thin film: forming a layer of inclusions in an initial substrate at a depth corresponding to the required thickness of the film (abstract). The inclusions are designed to form traps for gaseous compounds which are subsequently implanted to

Art Unit: 1791

(irreversibly) form micro-cavities and form a fracture plane along which the thin film can be separated from the remainder of the substrate (abstract). In one example for obtaining an SOI structure, on an initial substrate 31, a silicon film 32 (an intermediate layer), strongly doped with boron (extrinsic) atoms, is produced by epitaxy (column 12 lines 40-45, column 5 lines 10-12, figure 7). The substrate is then coated with an oxide film 34 (column 12 lines 45-50). The final structure 30 constitutes a plate as required by the claims. The substrate is then submitted to gaseous compound implantation (column 12 lines 51-54). The surface 35 of the substrate is bonded by wafer bonding to a silicon plate (a superstrate) (column 12 lines 55-57). Heat treatment is then performed to separate the structure 30 into two parts by means of a fracture at the inclusions zone in film 32 (column 12 lines 58-64). The presence of the (extrinsic) boron atoms implicitly causes the formation of micro-cavities (column 5 lines 20-21 and 30-33), and since the heat treatment induces fracture (weakening, rupture) of the substrate, it helps propagate (and further form) any cavities formed during the implantation step. Since micro-cavities are formed in film 32, and since film 32 is comprised of similar materials used by applicant as the intermediate layer, it is plastically deformable in the heat treatment range, and it is dielectric as required by the claims. The micro-cavities formed by this process implicitly constitute channels as required by the claims. Since the intermediate layer is formed by similar materials as used by applicant, and since it is doped with boron as described above, it is expected to form a borophosphosilicate glass as required by the claims.

***Claim Rejections - 35 USC § 103***

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

13. Claims 5, 8, 9, 15-17, 19, 29, 30, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moriceau et al. (WO 99/35674) as applied to claims 1-4, 7, 8, 12, 14, 18, 20, 31, and 33 above, and further in view of Haberger et al. (US 6,417,075). For the purposes of examination, (US 6,756,286) will be used as an English Language Equivalent for WO 99/35674.

14. As to claim 5, Moriceau does not appear to explicitly disclose chemically attacking the intermediate layer to cause separation. However, Haberger teaches in a method for producing thin substrate layers: separating two substrates by attacking an intermediate bonding layer in a wet chemical detachment process (abstract). It would have been obvious to substitute the chemical detachment process of Haberger with the

separation process of Moriceau as a conventional means for causing separation of silicon platelet 31 from the silicon plate (superstrate) bonded thereon (described above).

15. As to claim 8, Moriceau does not appear to explicitly disclose the use of phosphorus as a dopant for the intermediate layer. However, Haberger teaches in a method for producing thin substrate layers: the use of doped oxides such as PSG (phosphosilicate glass) or BPSG (borophosphosilicate glass) as the intermediate bonding layer in order to increase the etching rate in chip detachment (column 7 line 66 to column 8 line 3). To create a doped PSG or BPSG, phosphorus atoms or a mix of boron and phosphorus atoms respectively must be used as a dopant for the intermediate layer. It would have been obvious to substitute phosphorus, or a mix of boron and phosphorus, as the dopants for the intermediate layer as taught by Haberger with the boron dopant of Moriceau as an improvement to increase rate of detachment.

16. As to claim 9, Moriceau teaches that inclusions may be formed by a doping effect (column 5 lines 20-21 and 30-33). Moriceau further teaches that the degree of doping (with boron, or in the combination of references, with boron and/or phosphorus to make PSG/BPSG) has an effect on the formation of an inclusions zone (column 7 lines 24-45). A person having ordinary skill in the art would recognize that the degree of doping influences the formation of an inclusions zone, making it a result effective variable. Because it is a result effective variable and Moriceau teaches its optimization, it would have been obvious to optimize the degree of doping to attain the desired inclusions zone, and the claim is met.

Art Unit: 1791

17. As to claim 15, Moriceau does not appear to explicitly disclose chemically attacking the intermediate layer to cause separation. However, Haberger teaches in a method for producing thin substrate layers: separating two substrates by attacking an intermediate, sacrificial bonding layer in a wet chemical detachment process (abstract, column 4 lines 12-13, column 4 lines 20-24). It would have been obvious to substitute the chemical detachment process of Haberger with the separation process of Moriceau as a conventional means for causing separation of silicon platelet 31 from the silicon plate (superstrate) via the intermediate layer having micro-cavities formed therein (described above).

18. As to claims 16 and 17, Moriceau does not appear to explicitly disclose producing projecting portions in the substrate or superstrate on the intermediate layer side. However, Haberger teaches in a method for producing a thin substrate: forming a bonding (intermediate) layer having channel-shaped recesses in order to permit the penetration of an etching agent for subsequent separation (abstract, column 3 lines 63-66). The bonding layer with recesses formed therein/thereon is depicted at figures 1a and 1b. The formation of channel-shaped recesses constitutes the formation of rectilinear projecting portions extending to the sides of the intermediate layer (since it extends along the sides through the substrate depicted at figure 1). Since the substrates 1 and 2, and bonding layer 4 having channels 5, are formed into an integral structure at figure 1b, the bonding layer 4 is a part of the substrates 1 and 2, so the channels are also formed in the substrates as required by the claims (See MPEP 2144.04 V Section B). Alternatively, the channels can be formed in either substrate (column 4 lines 54-57).

It would have been obvious to apply the channels of Haberger as an improvement to the Moriceau method to allow for the penetration of a chemical etchant.

19. As to claim 19, Moriceau does not appear to explicitly disclose reducing the thickness of the superstrate and/or substrate. However, Haberger teaches in a method for producing a thin substrate: bonding two substrates to create a wafer stack, and thinning the wafer stack from one side down to the desired thickness (abstract, column 5 lines 5-10). It would have been obvious to apply the thinning method of Haberger to the method of Moriceau as an improvement to achieve a silicon wafer having the desired thickness.

20. As to claims 29 and 30, Moriceau does not appear to explicitly disclose producing projecting portions in the substrate or superstrate on the intermediate layer side. However, Haberger teaches in a method for producing a thin substrate: forming a bonding (intermediate) layer having channel-shaped recesses in order to permit the penetration of an etching agent for subsequent separation (abstract, column 3 lines 63-66). The bonding layer with recesses formed therein/thereon is depicted at figures 1a and 1b. The formation of channel-shaped recesses constitutes the formation of rectilinear projecting portions extending to the sides of the intermediate layer (since it extends along the sides through the substrate depicted at figure 1). Since the substrates 1 and 2, and bonding layer 4 having channels 5, are formed into an integral structure at figure 1b, the bonding layer 4 is a part of the substrates 1 and 2, so the channels are also formed in the substrates as required by the claims (See MPEP 2144.04 V Section B). Alternatively, the channels can be formed in either substrate (column 4 lines 54-57).

It would have been obvious to apply the channels of Haberger as an improvement to the Moriceau method to allow for the penetration of a chemical etchant.

21. As to claim 32, Moriceau does not appear to explicitly disclose reducing the thickness of the superstrate and/or substrate. However, Haberger teaches in a method for producing a thin substrate: bonding two substrates to create a wafer stack, and thinning the wafer stack from one side down to the desired thickness (abstract, column 5 lines 5-10). It would have been obvious to apply the thinning method of Haberger to the method of Moriceau as an improvement to achieve a silicon wafer having the desired thickness.

22. Claims 6 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moriceau et al. (WO 99/35674) as applied to claims 1-4, 7, 8, 12, 14, 18, 20, 31, and 33 above. For the purposes of examination, (US 6,756,286) will be used as an English Language Equivalent for WO 99/35674.

23. As to claim 6, the intermediate film 32 is formed of doped silica as described in the rejections above. Moriceau teaches that there are many deposition techniques chosen as a function of the materials to be prepared, which can be monocrystalline (column 5 lines 62-64). Moriceau does not appear to explicitly disclose that the silicon substrate/superstrate referred to in the rejections above is a monocrystalline silicon. It would have been obvious to substitute the materials taught by Moriceau to the make the silicon substrate 31 and superstrate of Moriceau from monocrystalline silicon as a conventional material used in the art for transferring a thin film of solid material.

24. As to claim 10, Moriceau teaches that inclusions may be formed by a doping effect (column 5 lines 20-21 and 30-33). Moriceau further teaches that the degree of doping (with boron) has an effect on the formation of an inclusions zone (column 7 lines 24-45). A person having ordinary skill in the art would recognize that the degree of doping influences the formation of an inclusions zone, making it a result effective variable. Because it is a result effective variable and Moriceau teaches its optimization, it would have been obvious to optimize the degree of doping to attain the desired inclusions zone, and the claim is met.

25. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moriceau et al. (WO 99/35674) as applied to claims 1-4, 7, 8, 12, 14, 18, 20, 31, and 33 above, and further in view of Aspar et al. (US 6,303,468). For the purposes of examination, (US 6,756,286) will be used as an English Language Equivalent for WO 99/35674. As to claim 11, Moriceau teaches that the heat treatment is determined based on the weakness of the inclusions layer (column 3 lines 60-62, column 4 lines 10-33). A person having ordinary skill in the art would recognize that the heat treatment influences fracture of the inclusions layer, making it a result effective variable. Because it is a result effective variable and Moriceau teaches its optimization, it would have been obvious to optimize the heat treatment to attain the desired fracture at the inclusions layer. Alternatively, Aspar teaches in a method for making at thin film: performing an annealing step between 0 to above 1000 °C on a layer having micro-cavities or micro-

bubbles in order to cause cleavage (by causing propagation of said cavities/bubbles) at that layer (abstract, column 3 line 65 to column 4 line 3).

26. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moriceau et al. (WO 99/35674) as applied to claims 1-4, 7, 8, 12, 14, 18, 20, 31, and 33 above, and further in view of Stierman et al. (US 4,979,015). For the purposes of examination, (US 6,756,286) will be used as an English Language Equivalent for WO 99/35674. As to claim 13, Moriceau does not appear to explicitly disclose that the silicon oxide layer 34 is a thermal oxide. However, Stierman teaches in a method for making an insulated substrate for an integrated circuit device: treating a deposited layer of silicon in a furnace to create a thermal silicon oxide insulating layer (column 4 lines 59-63). It would have been obvious to substitute the method for forming an oxide layer of Moriceau with the method of forming a thermal oxide of Stierman as a conventional alternative or substitutable method for depositing an oxide layer on a silicon substrate.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ATUL KHARE whose telephone number is (571)270-7608. The examiner can normally be reached on Monday-Thursday 7:30 a.m. - 5:00 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Christina Johnson can be reached on (571)272-1176. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ATUL KHARE/  
Examiner, Art Unit 1791

/Matthew J. Daniels/  
Primary Examiner, Art Unit 1791  
1/29/10